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Whale Optimization Algorithm for Performance Improvement of Silicon-On-Insulator FinFET

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ABSTRACT

Geometry parameters, fin height (H_{Fin}) & fin width (W_{Fin}), critically affect the performance of FinFET devices. These parametric variations have been assessed in the present work by designing silicon-on-insulator (SOI) fin-shaped field effect transistor (FinFET) device with optimum metrics. In this work, the designed devices show diminished Short channel effects and ameliorated analog parameters for the different range of H_{Fin} /L_g & W_{Fin}/L_g using 3D Visual Technology Computer-Aided Design (TCAD) simulator. Further after training the artificial neural network with a set of parameters and delineating the fitness function, genetic algorithm (GA) and Whale optimization algorithm (WOA) have been implemented. Corresponding to the minimal fitness function, a pair of optimized metrics has been provided in less time using the weighted sum approach. It is observed that the taller and wider fins serve the need of high I_{ON}, larger intrinsic gain and a better early voltage whereas narrow fin provides SCEs immunity for device. The results seized through optimization techniques are in good reconciliation with the results of Physical device simulator's with a deviation less than 7%.

Keyword: FinFET, Leakage current, SRAM, Subthreshold Swing, Whale Optimization Algorithm.

Mathematics Subject Classification: 90C15, 90-80

Computing Classification System: Hardware~Transistors;500, Mathematics of computing~ Evolutionary algorithms;500, Mathematics of computing~ Combinatorial optimization;500.

1. INTRODUCTION

In the era of downscaling, leading Semiconductor companies like Intel, Samsung, TSMC etc are formulating scaled FinFET (device of a vertical channel with the gate wrapped in different planes) in their processors due to its superior electrical characteristics, suppressed short channel effects, high drive current, low leakage current & better scaling capability (Schaller, 1997; Ho et al., 2013, Bhattacharya and Jha, 2014, Lee, 2016). For multifin SOI FinFET device, Ion/Ioff ratio in order of 10^{11}, leakage current in order of 10^{-19} for SiC3C and reduced Subthreshold Swing (58mV/dec) for GaAs as channel material has been obtained as compared to conventional devices (Kaur et al., 2017). SOI technology is preferred in low power and high switching applications due to diminished leakage path near the junction of source/drain regions. The exceptional SCEs such as DIBL and leakage current for designed FinFET structures are 15.8mV/V and 1.37e-17 A respectively (Aujla and Kaur, 2019). For

wireless communication system, Fully depleted SOI MOSFET is served as prominent device due to enhanced analog and RF performances such as higher cut-off frequency and improved transconductance (Raskin, 2019). The comparative analysis of partially depleted SOI, FD-SOI and bulk MOSFET devices along with the impact of HALO implantation on analog and RF process parameters has been done for the gate length of 0.08μm (Kilchytska et al., 2003). An improvement in transconductance, intrinsic gain, cut-off frequency and On/Off drain current ratio has been obtained for scaled trigate bulk FinFET device (bha et al., 2019). Moreover, fully-depleted (FD) SOI MOSFET is an appropriate device for analog applications as it results in high transconductance to drain current ratio and this advantage can make them to work efficiently at high temperature or at high frequency (Colinge, 1998).

Utilization of Meta-heuristic approaches for designing and optimization of engineering problems has appeared as a significant tool in obtaining optimum process parameters. Because they do not require gradient information, can bypass local optima and easy to implement (Mirjalili and lewis, 2016).The electrical characteristics of 20nm bulk FinFET with triangular shaped fin have been optimized using artificial neural network (ANN) and Genetic algorithm (GA). It was demonstrated that the performance metrics viz. Drain induced barrier lowering (DIBL), leakage current, drive current has been improved after optimization (Gaurav et al., 2016). The device optimization using Whale optimization Algorithm (WOA) has also been done due to its less convergence time as compared to others algorithms (Mukherjee et al., 2017).Traffic path planning system has been implemented with the modified Fuzzy cognitive maps (Vascak, J., 2012). A novel gas optimization algorithm has been demonstrated with benchmark functions and showed improved efficiency w.r.t GA and particle swarm optimization (PSO) algorithms (Shams et al., 2017). An optimum Traffic Light system has been realized with modified Fuzzy model (Gil et al., 2018). An efficient novel algorithm based on search and rescue operation has been proposed for real world applications (Shabani et al., 2019).Fuzzy controlled system has been created using several advanced nature inspired algorithms (Precup and David, 2019).

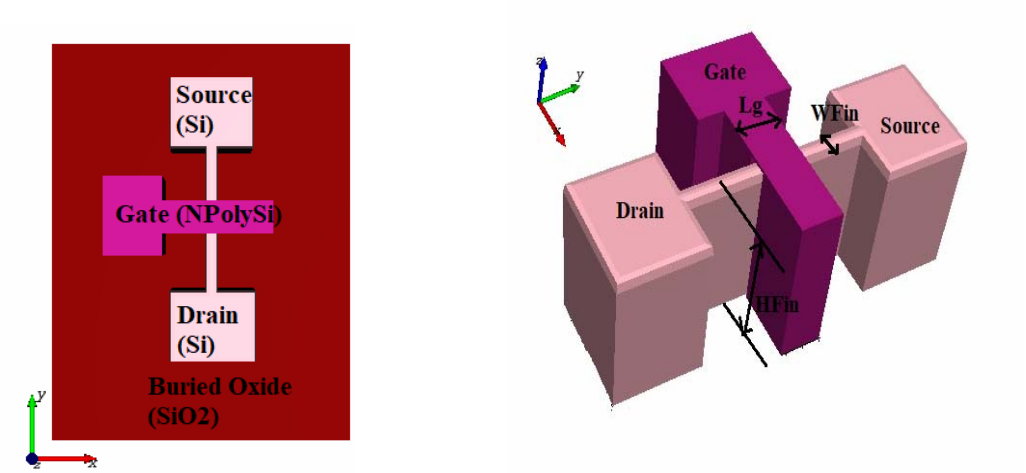
Research on the development of FinFET is on-going at 10 nm and even 7 nm technology node (Kang et al., 2013; Eneman et al., 2013). However, no systematic design guideline for the design of the channel and source/drain contact has been presented. Hence this article is focused on design of 14nm SOI FinFET using GA and WOA optimization techniques.

This paper is arranged as follows: Section 2 discusses the device design and the Simulation framework. The analysis of FinFET performance using metrics like SCEs and analog parameters are indicated in the section 3. Device optimization using GA and WOA via ANN and the summary comparison of MATLAB and TCAD results with previous literature are demonstrated in section 4. Section 5 concludes the work done.

2. DEVICE DESIGN AND SIMULATION FRAMEWORK

The structure of the vertical body profile in the n-channel region SOI FinFET is shown in Figure 1. A FinFET with SiO_2 as interfacial oxide and N-poly-silicon as a gate electrode in underlap regions has been modeled. The design considerations of the device are shown in Table 1. The doping

concentration for channel, source/drain and substrate are 10^{17} cm^{-3}, 3×10^{20} cm^{-3} and $1x10^{16}$ cm^{-3} respectively. The gate work function for the device is 4.5 eV at 300K temperature and the thickness of SiO_2 as gate dielectric and buried oxide is 1nm and 20nm respectively (Colinge, 2008; Sun et al., 2011)



(a) (b)

Figure 1. Bird eye views of designed SOI FinFET devices(a) 2-D view (b) 3D view with device dimensions

Table 1 : Process Parameters of designed FinFET

Design Parameters	**Intel***	**Present work**
Gate length, L_g (nm)	14	14
Oxide thickness, T_{ox} (nm)	1.0	1.0
Supply Voltage (V)	0.8	0.7

**as per ITRS dimensions (2013),http://public.itrs.net*

Table 2 : Typical Cases Taken For Simulation

Design Parameters (Colinge, 2008; Ho et al., 2013; Sun et al., 2011, Mohapatra et al., 2015)	**H_{Fin}/L_g**	**W_{Fin}/L_g**
	0.72,1.43,2.15,2.9,3.58	0.36,0.5, 0.65,0.79,0.93,1,1.08

Typical cases of W_{Fin}/L_g and H_{Fin}/L_g for simulation of designed device are mentioned in Table 2. The proposed device is designed, simulated and analyzed using Cogenda Visual TCAD. The device is designed using GDS and process file and the file obtained through this process is in tif3D format. The process file involves the description of the device structure including the doping profiles, electrical contact, meshing and material regions. The simulator adopted various physical models viz. Drift Diffusion, Lucent mobility, Band-to-Band tunnelling, along with Shockley–Read–Hall (SRH) and Auger recombination models for solving diffusion and transport equations .Further, the device performance

parameters are extracted and their analysis has been done using numerical methods (Kaur et al., 2019 ; Mohapatra et al., 2015 ; De Andrade et al., 2012). The validation of simulator has been examined by comparing TCAD results with existing research work. Figure 2 illustrates that the simulation results are in good agreement with the published work (De Andrade et al., 2012). Figure 3, demonstrates the V-I characteristic of the device at the drain voltage of 0.7V and 50mV with gate ramp from 0 to 0.7V. It is depicted that higher drain voltage (0.7V) has more drive current as compared to corresponding drain voltage of 50mV. The output characteristic curve of the device is shown in Figure 4 in which graph is plotted for 0.7V and 50mV gate voltages with corresponding ramp drain voltages from 0 to 0.7V.

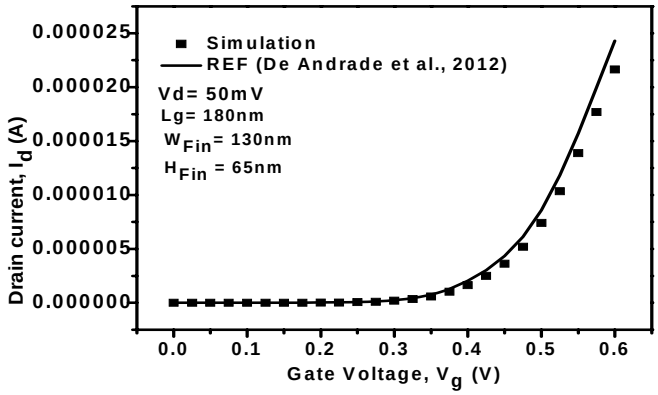


Figure 2. Identical I_d-V_g simulation results of designed FinFET structure with reference results (De Andrade et al., 2012)

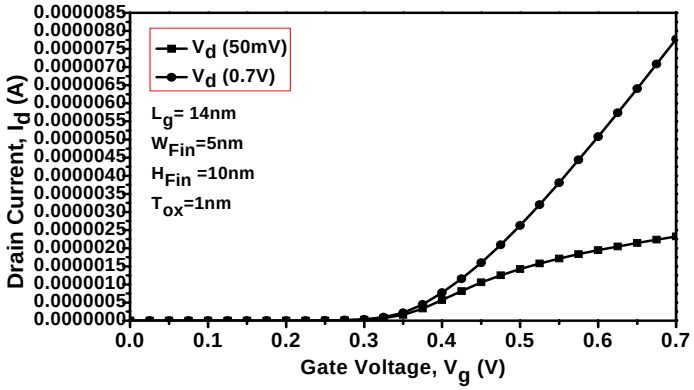


Figure 3. V-I characteristic curve in Linear and saturation region of designed FinFET device

3. FINFET PERFORMANCE

The impact of device fin parameters (W_{Fin}/L_g and H_{Fin}/L_g) variation on various performance metrics such as short channel effects viz. on-current or drive current (I_{ON}), off-current or leakage current (I_{OFF}), the ratio of I_{ON} and I_{OFF} (I_{ON}/I_{OFF}), Subthreshold Swing (SS) and analog parameters viz. Transconductance (g_m), Transconductance Generation Factor (TGF), output conductance (g_d), intrinsic gain (A_v) and early Voltage (V_{EA}) are presented systematically.

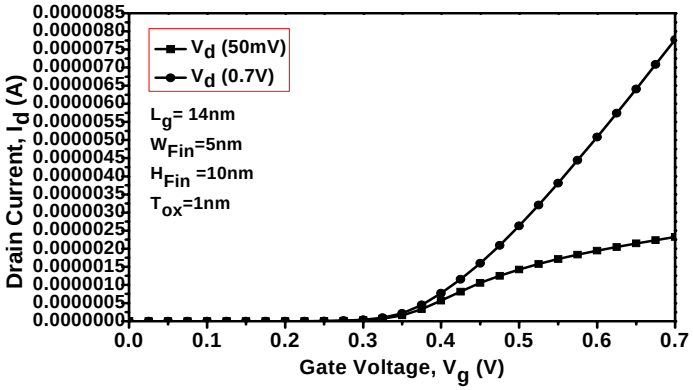


Figure 4. Output characteristics of SOI FinFET device

3.1. Effects of Fin Height

The drive current is defined as the value of current calculated at V_d= 50mV and V_g= 0.7 V. Leakage current is referred as current value when applied input gate voltage is zero (V_g= 0V).Subthreshold Swing (*SS*) is the inverse of sub-threshold slope (*S*); it is stated as the ratio of change in applied gate voltage to the decade change in drive current.

$$SS = \frac{\partial V_g}{\partial \log_{10} I_d} \tag{1}$$

The performance parameters I_{ON}, I_{ON}/I_{OFF} ratio and *SS* are calculated for designed devices as shown in Figure 5 and 6 .From Figure 5 it is observed that higher drive current is obtained for increased Fin height where as in Figure 6 reduction of on-off current ratio occur because of enhancement of leakage current with increased fin height. The better *SS* is required for the high speed switching capability of device for digital circuits. The *SS* presented in Figure 6 is near to ideal value i.e. 60mV/dec at 300K (Sakhi and Chowdhury, 2013), also it is observed that *SS* is less affected by fin height variation, it fluctuates between 62.5mV/dec to 62.8 mV/dec. This happens because of the structure of FinFET device, as the gate is wrapped from three sides of channel with thin Fin width. Therefore, the device has more immunity to SCEs and greater electrostatic control over the channel.

Transconductance (g_m) can be calculated by taking the ratio of variable drain current (∂I_d) to the variable gate voltage (∂V_g) at constant value of drain source voltage (V_d). Basically, g_m represents its capability of converting input voltage change into output current. It also describes the switching capability of device, which means that higher the transconductance, faster the device can switch on and off. Therefore, higher clock frequencies can be supported for this type of device. Figure 7 show the trend of the variation of transconductance ($g_m = \partial I_d / \partial V_g$) and transconductance generation factor (g_m/I_d) w.r.t gate voltage for fin height 10nm and fin width 5nm. Both g_m and I_d are increasing with the increase in H_{Fin}/L_g ratio of the designed devices, extracted g_m for height variation is presented in Figure 8. For producing higher drive current, taller fins are preferred whereas for reduced SCEs, thin fin is required because it may reduce the cause of an electric field in silicon surface which further lessen I_{OFF}. The decreased g_d is detected in Figure 9 for lower H_{Fin} for designed device. CMOS based

analog circuits require transistors with low value of output transconductance ($g_d=\partial I_d / \partial V_d$) and high value of gain. Both are obtained for the case of low fin height ratio i.e. 1.43 and high H_{Fin}/L_g= 2.9 respectively. Further, TGF is directly proportional to g_m and is suitable for the realization of analog circuits at low voltage supply. Due to brevity, the extracted values of higher intrinsic gain (A_V= 20*$\log_{10}$ (g_m/g_d)) and early voltage (V_{EA}= I_d/g_d) are 125dB and 3.7V respectivley, achieved at the lower fin height of 10nm (Sun et al., 2011 ; Mohapatra et al., 2015)

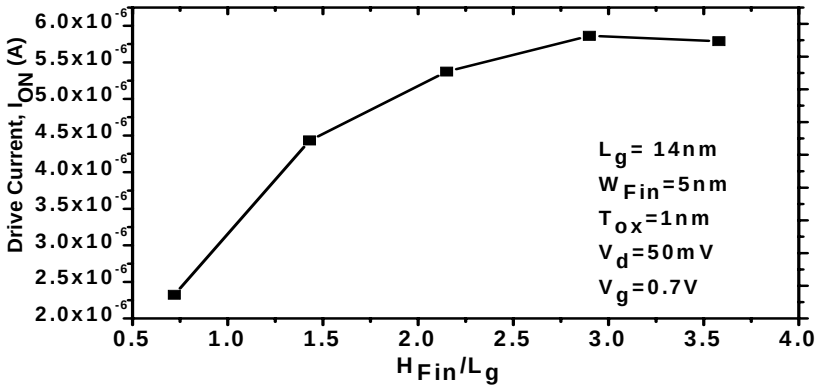


Figure 5. I_{ON} variation w.r.t H_{Fin}/L_g for FinFET device.

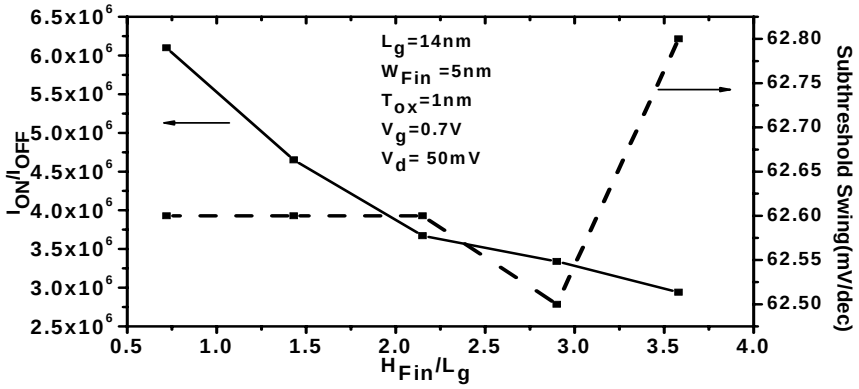


Figure 6. *SS* and I_{ON}/I_{OFF} variation w.r.t H_{Fin}/L_g for FinFET device.

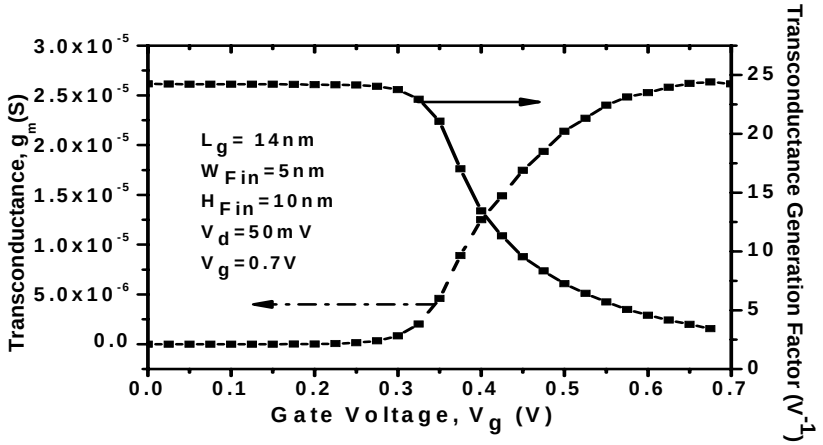


Figure 7. Gate voltage versus g_m and *TGF* for FinFET device

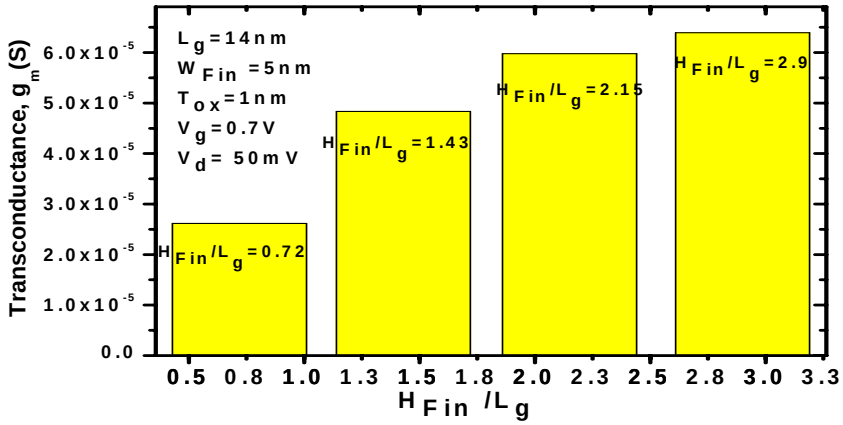


Figure 8. Transconductance for H_{Fin}/L_g variation.

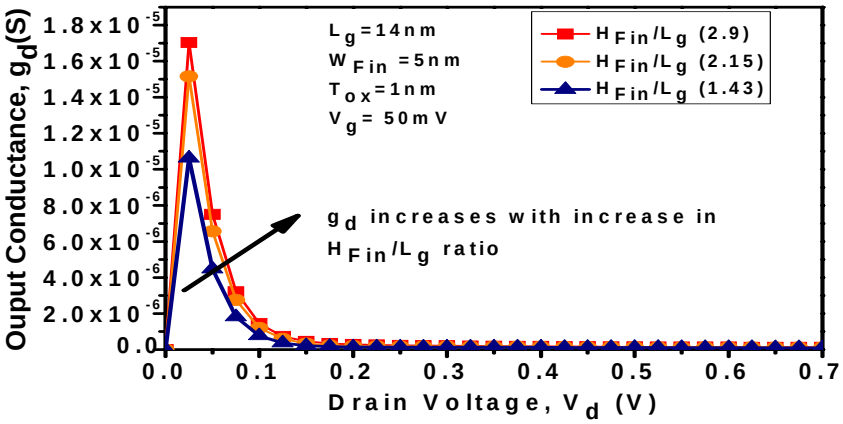


Figure 9. Drain voltage versus output conductance for H_{Fin}/L_g variation.

3.2. Effect of Fin Width

The sensitivity of fin width for I_{ON}/I_{OFF} and *SS* of designed device is shown in Figure 10. Here, it is observed that for high fin width, SCEs arises because of larger longitudinal electric field at the source side and larger distance between multiple gates, which in turns leads to high leakage current, *SS* and reduced I_{ON}/I_{OFF}. Therefore, it is depicted that for SCEs immunity narrow fin width is suitable. The analog parameters like *TGF* and V_{EA} are plotted for W_{Fin}/L_g variation in Figure 11 and 12. Larger *TGF* is required for producing highly efficient device. It is predicted that higher value of *TGF* is obtained at least W_{Fin}/L_g as shown in Figure 11. *TGF* is dependent parameters of transconductance, which further depends on I_d. More drive current is demonstrated for larger fin width because of immense accommodation of charge carriers in the larger area of the device. Better early voltage (V_{EA}) is demonstrated for lower value of W_{Fin}/L_g, because of reduction in substrate effects, body heating effects and higher immunity towards SCEs. The g_d shows degradation by the order of 10^4 for increased fin width of the device (Mohapatra et al., 2015 ; Nandi et al., 2013).

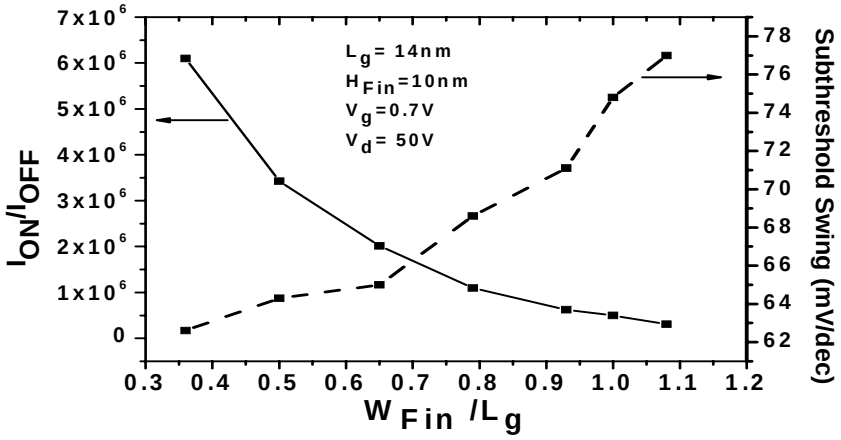


Figure 10. I_{ON}/I_{OFF} and *SS* variation w.r.t W_{Fin}/L_g for FinFET device.

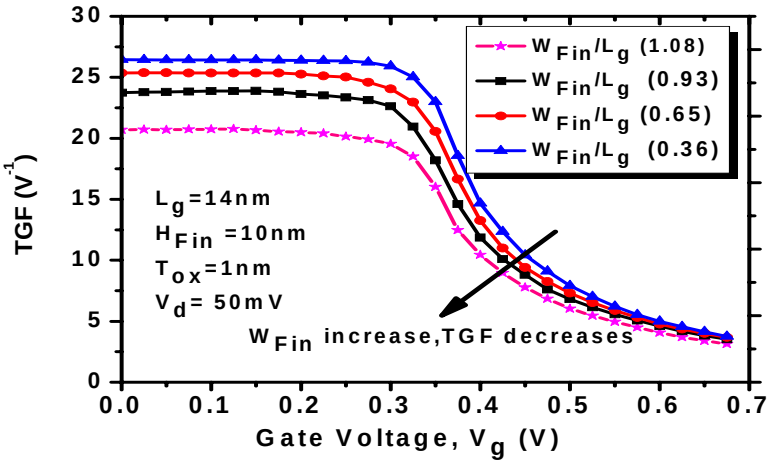


Figure 11. *TGF* variation for different W_{Fin}/L_g ratios

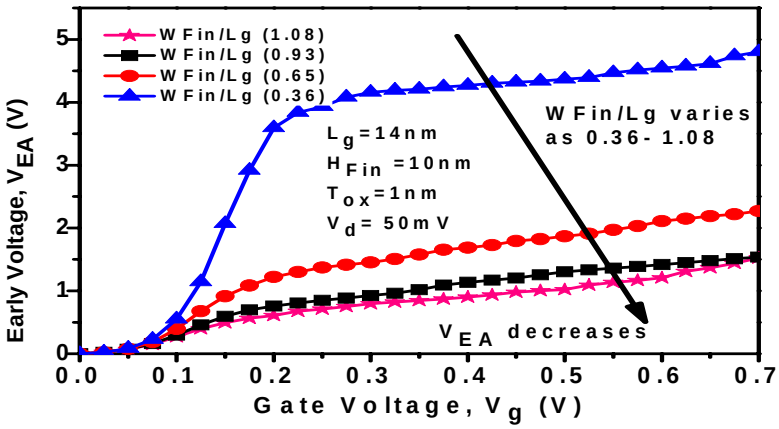


Figure 12. V_{EA} variation for different W_{Fin}/L_g ratios

4. PARAMETER OPTIMIZATION WITH GA AND WOA through ANN Training

4.1. Training of Artificial Neural Network

ANN is defined as a computing system which consists of highly interconnected multiple neurons which mimic the biological behaviour of human brain. The multilayer feed-forward model of neural network contains three interconnected layers: an input, an output and the hidden layer as shown in Figure 13.The input layer brings the input signal into system through consecutive layers of neurons for further processing. The intermediate hidden layer solves the desired problem using sigmoid transfer function (activation function) and a set of associated weighted inputs. The output layer produces the output of the network using linear transfer function. In this way, ANNs can be trained by amending the weight values of interconnected neurons.The given network is trained with Levenberg-Marquardt backpropagation algorithm (trainlm).TRAINLM is preferred because it require less memory and has more speed as compared to other algorithms. Although, this algorithm provides training with validation and test vectors and also its network has derivative functions for their transfer function, weight and net input. Backpropagation is used to calculate the Jacobian *'jX'* of performance *'perf'* with respect to the weight and bias variables *'X'*. Each variable is adjusted according to Levenberg-Marquardt equation,

$$jj = jX * jX \quad 2(a)$$

$$je = jX * E \quad 2(b)$$

$$dX = -(jj + I * mu)je \quad 2(c)$$

where E is all errors and I is the identity matrix (Hagan and Menhaj, 1994; Sapna et al., 2012) Training is stopped after satisfying few of conditions viz. Maximum number of epoches (repetitions) is reached, Performance is minimized to the goal etc.

i). Through ANN network, two input elements (W_{Fin} & H_{Fin}) and five output elements (*SS,* I_{ON}, g_m, V_{EA} *& TGF*) has been created with 20 hidden neurons by giving 70 data samples for optimizing FinFET parameters. As each input have corresponding five output parameters in the output dataset.

ii). Separately created datasets for device has been applied to NN (Neural Network) Toolbox of MATLAB for obtaining the required net files. The total data samples considered for training the network has been divided as 70% (48 samples) for training samples, 15% (11 samples) for validation and remaining 15% (11 samples) for testing samples. After finishing the training process, mean squared error (mse) of the trained network is 0.10125 obtained at the 8^{th} epoch is shown in Figure 14. MSE determines the network's performance and is measured as an average squared difference between targets and outputs. Through ANN network, two input elements (W_{Fin} *&* H_{Fin}) and five output elements (*SS,* I_{ON}, g_m, V_{EA} *& TGF*) has been created with 20 hidden neurons by giving 70 data samples for optimizing FinFET parameters. As each input have corresponding five output parameters in the output dataset.

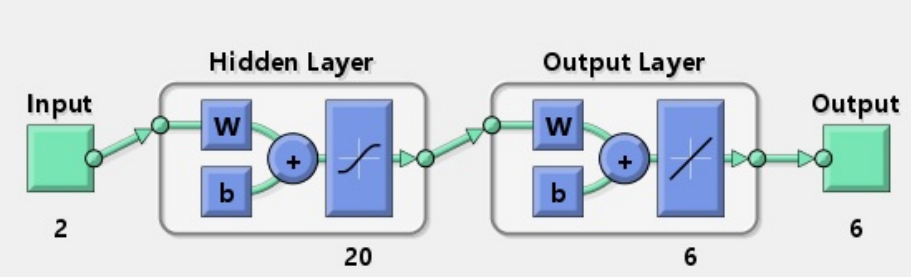


Figure 13. ANN Architecture

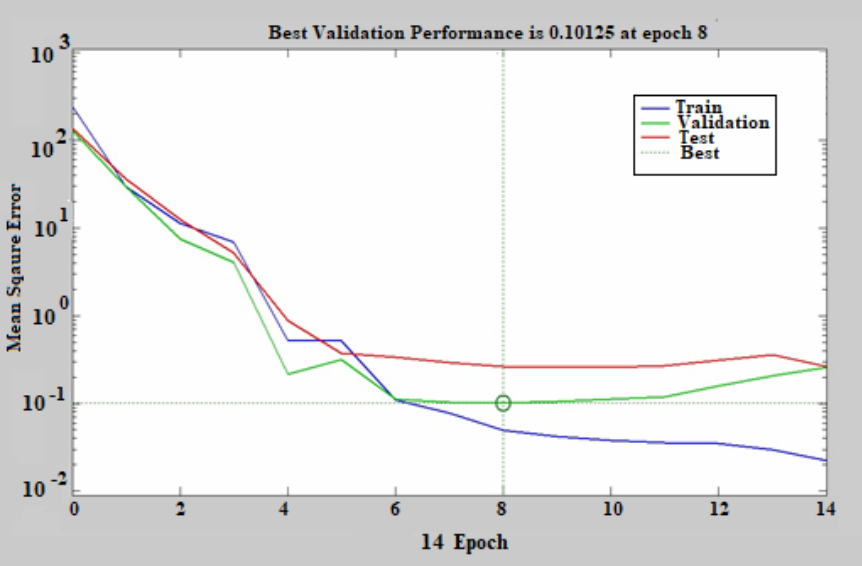


Figure 14. Performance of Levenberg-Marquardt Backpropagation Algorithm

iii).Separately created datasets for device has been applied to NN (Neural Network) Toolbox of MATLAB for obtaining the required net files. The total data samples considered for training the network has been divided as 70% (48 samples) for training samples, 15% (11 samples) for validation and remaining 15% (11 samples) for testing samples. After finishing the training process, mean squared error (mse) of the trained network is 0.10125 obtained at the 8^{th} epoch as shown in Figure 14. MSE determines the network's performance and is measured as an average squared difference between targets and outputs. The value is nearer to zero which indicates improved performance for device. Another measuring parameter is Regression (R) which is defined as the correlation between targets and the output. The regression values for FinFET device is: Training = 0.99999, Validation=0.99983, Testing= 0.99983 and all=0.99994 as outlined in Figure 15. R near to 1 value shows close relationship between target and output (https://in.mathworks.com/discovery/neural-network.html).The results obtained by improved trained networks are saved in MATLAB and further used for optimization (Aujla and Kaur, 2019; Kipli et al., 2012).

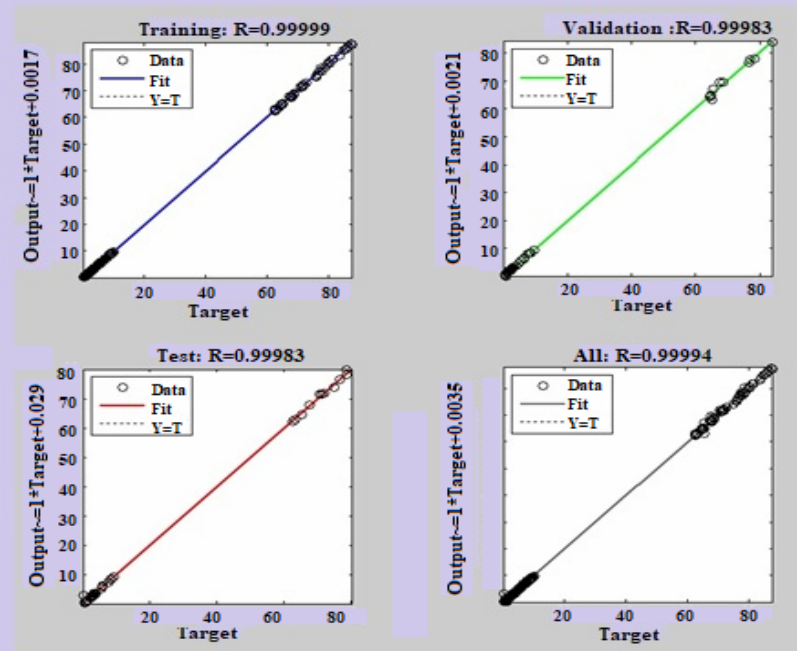


Figure 15. Regression Analysis Plot for Levenberg-Marquardt Backpropagation Algorithm

4.2. Optimizing Algorithms

In the present research, a single objective function has been used for optimizing FinFET parameters which produces a single global optimal (minimum) value. The objective function '*f*' for the defined problem (optimized fin width and fin height) of device is given as

$$f = SS - I_{ON} \times 10^{6} - g_m \times 10^{5} - V_{EA} - TGF \times 10^{-1} \quad (3)$$

where *SS* is Subthreshold Swing (mV/dec), I_{ON} denotes drive current (A), g_m (S), indicates Transconductance, Early voltage is V_{EA} (V) and *TGF* is Transconductance generation factor measured as V^{-1}. In order to attain the optimized parameters, the objective function mentioned in equation (3) is required to be reduced through optimization algorithms such as Genetic Algorithm and Whale Optimization Algorithm.

4.2.1. Genetic Algorithm

GA is a heuristic search algorithm used in artificial intelligence and computing. It is based on the concept of natural selection where the fittest individual are selected for producing optimum results for the defined problem with fitness function, '*f*' as mentioned in equation (3).The constraints given as input to GA for the defined problem are : Lower bounds = [5 10] ; Upper bounds= [15 55]. The main operators of this algorithm are mutation, selection and crossover. To perform these operations, the selected population type is 'double vector' due to the integer constraints. The initial size of population is selected as 40 and the 'rank' has been chosen as fitness scaling function for generation of new population of individuals. The 'rank' of individual represents its location sorted in increasing order

instead of its raw score. The 'stochastic uniform' selection function has been used for selecting parents for generation of new offsprings. The Probability values of '0.8' for crossover and '0.2' for mutation have been used for generation of new offsprings. Migration defines how an individual moves between subpopulation numbers (https://in.mathworks.com/discovery/genetic-algorithm.html). The stopping criteria for this algorithm includes number of generations (taken as 100) and function tolerance (a point where a weighted average change in fitness function is less than the function tolerance of 10^{-12} (Aujla and Kaur, 2019).The optimal input and output parameters of FinFET obtained through GA toolbox have been mentioned in Table 3.

4.2.2. Whale Optimization Algorithm

WOA algorithm imitates the hunting behaviour of humpback whales. This algorithm begins with the random population of whales. These whales find the optimum position of prey's and attack them using one of these methods.

(i) Encircling technique: The whales update their location depending upon best position as given in equation (4) and (5)

$$D = \left| C \otimes X^*(t) - X(t) \right| \tag{4}$$

$$X(t+1) = \left| X^*(t) - A \otimes D \right| \tag{5}$$

D is the distance between prey and whale, $X^*(t)$ indicate whale earlier best position and $X(t+1)$ is the whale current position. The coefficient vectors, 'A' and 'C' are defined as follows:

$$A = 2a \otimes r - a \tag{6}$$

$$C = 2r \tag{7}$$

where r is a random vector having range [0,1] and the value of 'a' decreases from 2 to 0 as the iterations proceed. The value of 'A' and 'C' coefficients lie between [-2, 2] and [0, 2].

(ii) Bubble-net attacking technique: This technique contains two methods. The first method includes the shrinking encircling, which can be explained by diminishing the variable 'a' and also 'A' as quoted in equation (6). The second is the spiral updating position. This activity of whales for making spiral shape around prey can be expressed as:

$$X(t+1) = D' \otimes e^{bl} \otimes \cos(2\pi l) + X^*(t) \tag{8}$$

$D' = \left| X^*(t) - X(t) \right|$ is the difference between humpback whale and prey, 'b' is a constant variable, $\otimes$ represents element-by-element multiplication and 'l' is random variable with range = [-1,1].

The probability of 50% is taken as an assumption for choosing either of two methods for catching the prey during iterations of the algorithm. The whales can swim around the prey along a spiral-shaped path and at the same time the circle shrunk using as follows:

$$X(t+1) = \begin{cases} X^*(t) - A \otimes D & p \geq 0.5 \\ D' \otimes e^{bl} \otimes \cos(2\pi l) + X^*(t) & p < 0.5 \end{cases} \tag{9}$$

where 'p' is a random probability value lies between 0 and 1. The randomness of probability make effective transition between exploration and exploitation phases. It interprets the probability of deciding either of the spiral model or the shrinking encircling method to adjust the position of whales.

(iii) Search for prey : In this method, the whales randomly searches the position of prey instead of the best search agent as follows :

$$D = \left| C \otimes X_{rand} - X(t) \right| \quad (10)$$

$$X(t+1) = \left| X_{rand} - A \otimes D \right| \quad (11)$$

X_{rand} is randomly search position vector.

(https://in.mathworks.com/matlabcentral/fileexchange/55667-the-whale-optimization-algorithm).

The defined fitness function *'f'* quoted in equation (3) has been applied to WOA algorithm for optimizing the parameters of designed FinFET. The WOA started randomly with population size of 40 in search domain of input elements : height and width range of [10 55] and [5 15] respectively for 100 iterations. For each pair of input parameters, the fitness function mentioned in equation (3) is calculated for best solution. The *'A'* and *'C'* parameters are determined depending on decreased value of *'a'* and better solution is updated based on probability metric *'p'*.The preceding steps are repeated until stopping criteria is reached (number of iterations=100) and optimized parameters are obtained as shown in Table 3 Therefore, WOA algorithm has the capability of providing high local optima avoidance and convergence speed over the course of iterations. WOA algorithm converges earlier as compared to GA algorithm because it eliminate the problem of staying in local optima and hence the speed of WOA algorithm incresed with respect to others. The flowchart for WOA operation is shown in Figure 16.

WOA converges at 8^{th} iteration and whereas GA converges at 17^{th} iteration for FinFET device with lesser time i.e.51s (approx.) as compared to GA as shown in Table 3 (Aziz et al., 2018 ; Mathworks, 2020) and in Figure 17. The source code of WOA is available at http://www.alimirjalili.com/WOA.html.

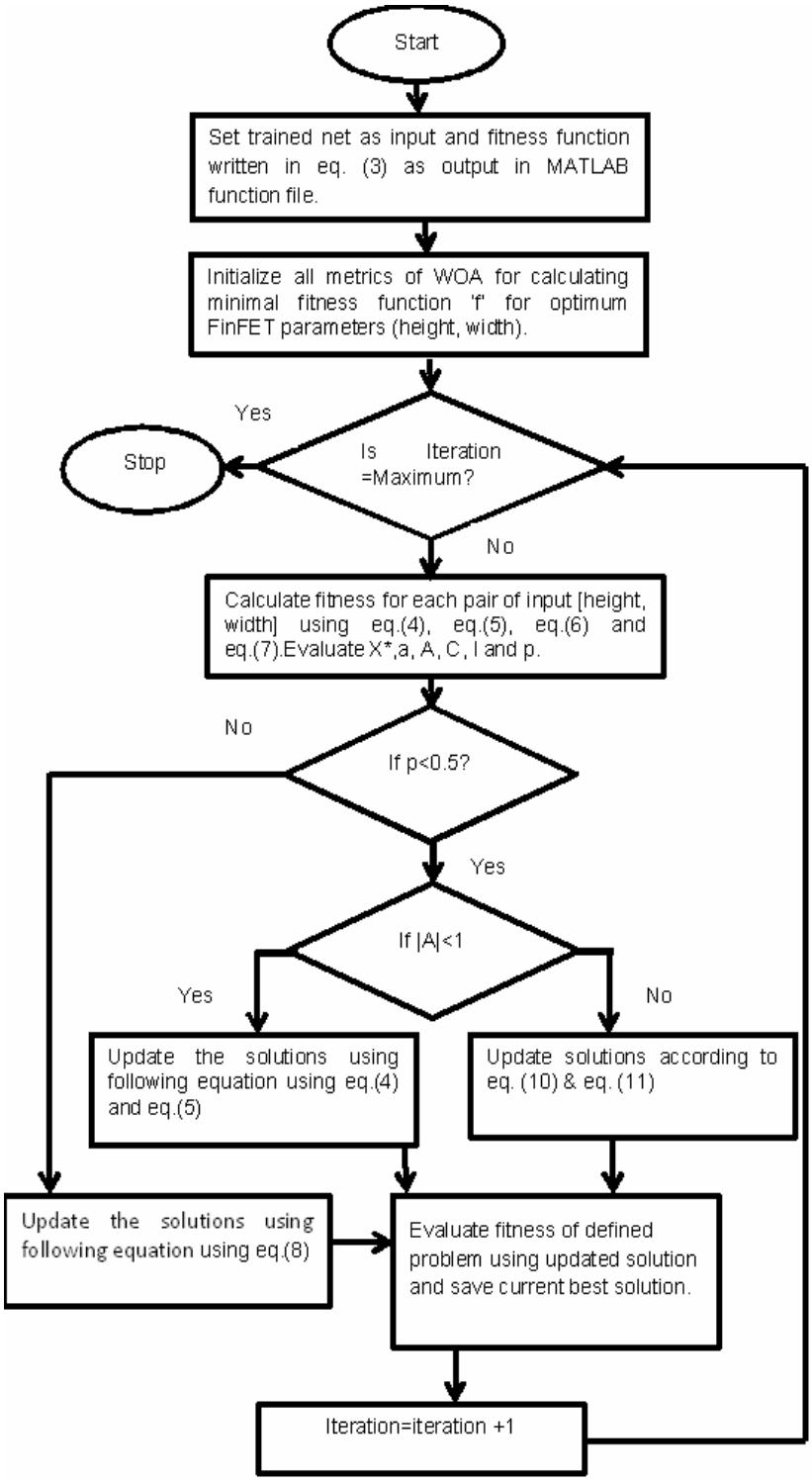


Figure 16. Flowchart for WOA operation

Table 3 : Optimized Input parameters obtained through GA and WOA for FinFET

Applied Algorithm in MATLAB	Total Function Evaluations	Optimum fitness function, f	Output Parameters	Input Parameters	Time
Genetic Algorithm	4000	47.662	I_{ON}=6.0542 X 10^{-5} A ***SS***= 62.7092 mV/dec g_m =3.1474 X 10^{-5} A V_{EA}=3.433 V ***TGF***= 24.123 V^{-1}	W_{Fin} =5nm H_{Fin} =45nm	64.367 sec
Whale Optimization Algorithm	4000	47.662	I_{ON}=6.0542 X 10^{-5} A ***SS***= 62.7091 mV/dec g_m =3.1474 X 10^{-5} A V_{EA}=3.433 V ***TGF***= 24.123 V^{-1}	W_{Fin}=5nm H_{Fin} =45nm	50.972 sec

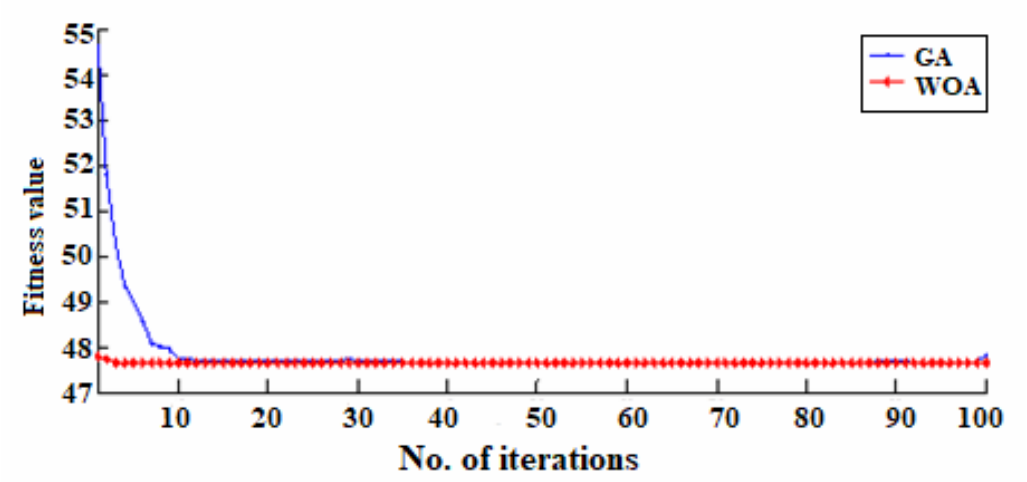


Figure 17. Convergence Curves for both devices created through GA and WOA algorithms

The comparison of results obtained through MATLAB optimizing tools (GA & WOA) and TCAD has been mentioned in Table 4. MATLAB provides two optimal input metrics viz. Height =45nm & width=5nm and their corresponding output parameters such as I_{ON}, *SS*, g_m V_{EA} and *TGF*. The same input dimensions has been used for designing a optimal FinFET device in TCAD tool. Then, the difference between output parameters result obtained through MATLAB and TCAD has been evaluated in terms of percentage change in order to validate the tool. The results obtained after applying optimization tool to a proposed device are compared with previous literature. It is observed that the designed device illustrate the improvement for analog parameters and have comparable values of I_{ON} & g_m, along with reduced leakage current, output transconductance and higher value of early voltage as compared to previous work.

Table 4 : Verification of Optimized results and comparison of obtained optimized results with existing work

Proposed FinFET ***(L_g= 14nm,W_{Fin}= 5nm, H_{Fin}= 45nm, T_{ox}=1nm, V_g=0.7V, V_d=50mV)***			**FinFET** ***(L_g= 20nm, W_{Fin}= 10nm, H_{Fin}= 26nm, T_{ox}=0.9nm, V_d=V_g=0.7V)*** **(Han, 2017)**	**SOI FINFET** ***(L_g= 14nm, W_{Fin}= 8nm, H_{Fin}= 26nm, T_{ox}=1nm, V_d=V_g=0.9V)*** **(Lee, 2016)**
MATLAB	**TCAD**	**Percentage change (%)**		
I_{ON}=6.0542 X 10^{-6} A	I_{ON}=5.78 X 10^{-6} A	4.51	I_{ON}=0.35 X 10^{-6} A	I_{ON}=14 X 10^{-5} A
SS=62.7092 mV/dec	***SS***= 62.7 mV/dec	0.014	----	***SS***=77.562.7 mV/dec
g_m =3.1474 X 10^{-5} S	g_m =2.9406 X 10^{-5} S	6.57	g_m =10 X 10^{-5} S	----
V_{EA}=3.433 V	V_{EA}=3.444 V	0.31	V_{EA}=1V	----
TGF= 24.123 V^{-1}	***TGF***= 24.247 V^{-1}	0.514	----	----
----	I_{OFF}= 1.84 X 10^{-12} A	----	I_{OFF}= 0.5 X 10^{-12} A	I_{OFF}= 1 X 10^{-9} A
----	g_d =5.4 X 10^{-12} S	----	g_d =10 X 10^{-8} S	----

5. CONCLUSION

This research work provides a comprehensive analysis of geometry parameters variations for designing a FinFET device. The device with larger dimensions have higher I_{ON} and g_m and have lesser Leakage current, I_{ON}/I_{OFF} and *SS* because of limited control of gate over channel. Therefore, it is summarized that for high drive current taller fin height is suitable whereas for reduced SCEs narrow fin width is preferred. The impact of fluctuations of H_{Fin}/L_g and W_{Fin}/L_g shows that for better performance in terms of intrinsic gain, early voltage, TGF and output conductance the device dimensions should be reduced. Population based evolutionary algorithms GA and WOA have effectively maximized the performance of device by giving optimized performance metrics for particular fin height and fin width. The optimized dimensions created by algorithms are utilized for designing a device in TCAD and its process parameters are evaluated and compared to check the validation of the simulator. With this, it is concluded that the valuable results obtained from designing of multigate underlap SOI FinFET device could satisfy the need of low power standby applications. Further, for future scope the techniques like spacer engineering; work function variation; channel material variation etc. can be applied to proposed device for getting better performance of device and their application in memory circuits.

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